All DØ Meeting, August 3, 2001, Fermilab

Track & PreShower L1 Digital Trigger

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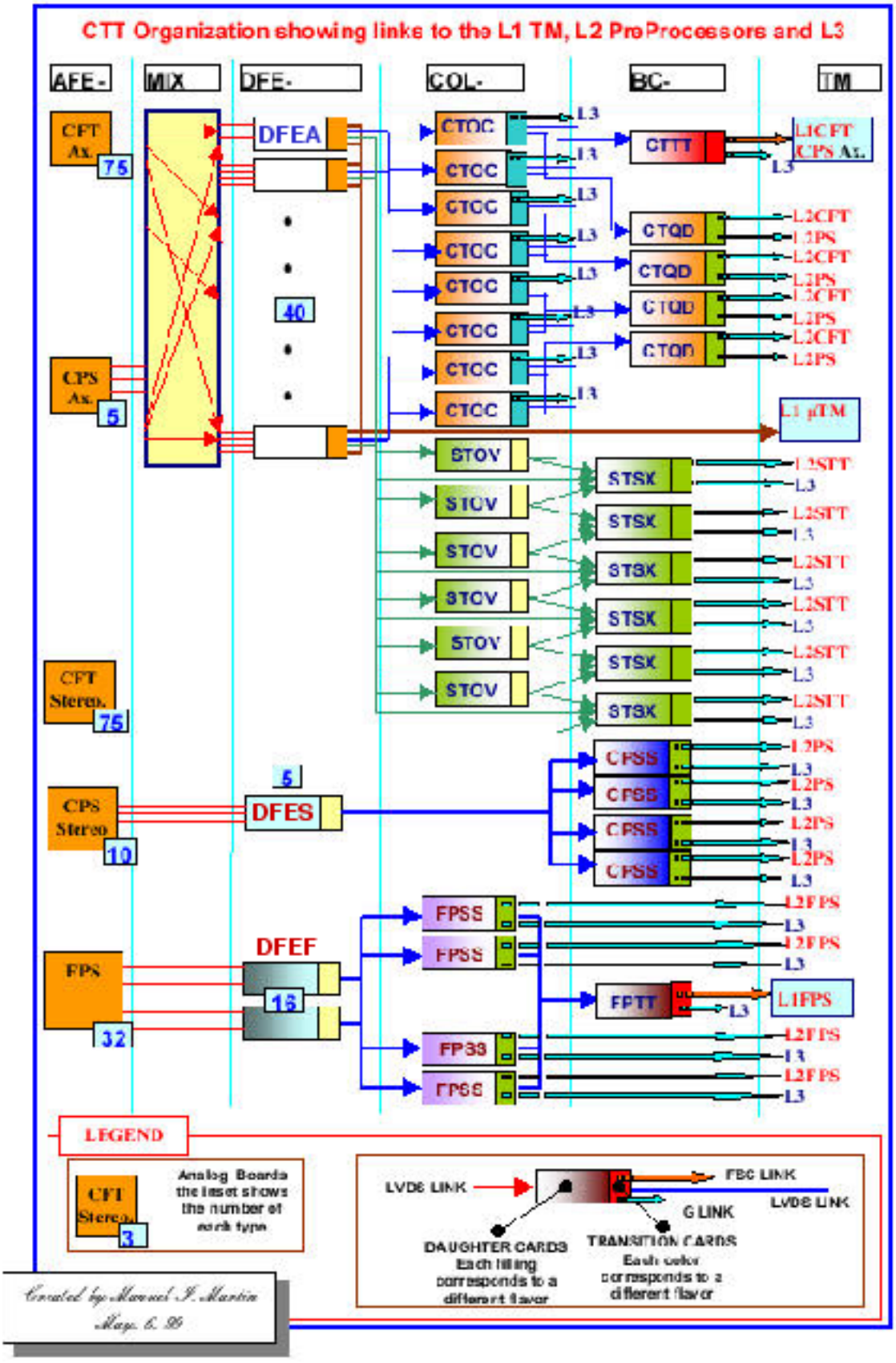
http://www-d0.fnal.gov/~blevan/upgrade.html

Introduction

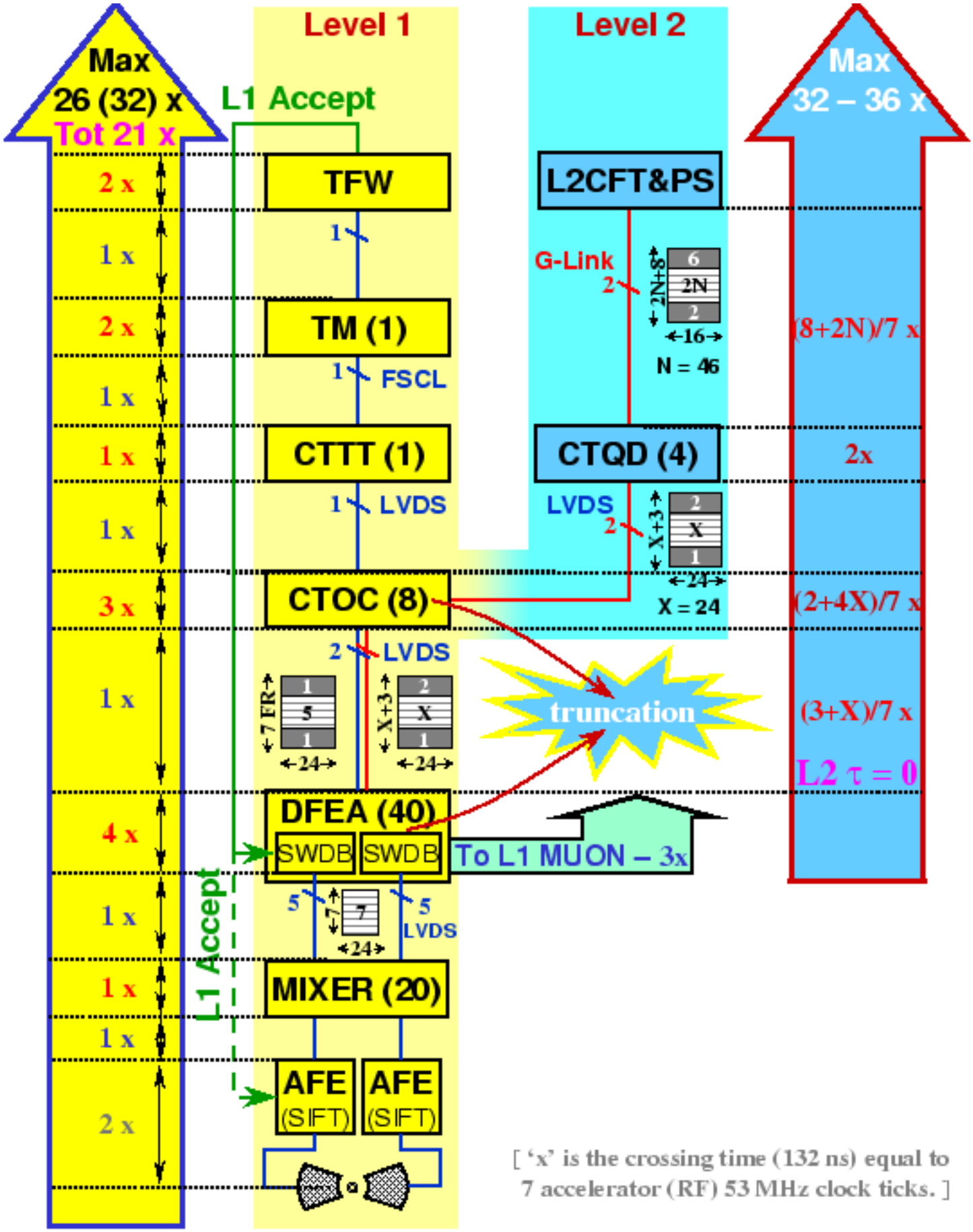

CTT Organization showing links to the L1 TM, L2 PreProcessors and L3
AFE-
MIX
DFE-
COL-
BC-
TM
CFT Ax.
75
CPS Ax.
5
DFEA
40
CTOC
CTTT
L1CFT
CPS Ax.
CTQD
L2CFT
L2PS
L3
L1 µTM
STOV
STSK
L2STT
CFT Stereo.
75
CPS Stereo
10
5
DFES
CFSS
L2PS
FPS
32
DFEF
16
FPSS
FPTT
L1FPS
FP33
FP66
L2FPS
LEGEND
CFT Stereo.
3
Analog Boards the label shows the number of cards type
LVDS LINK
FEC LINK
LVDS LINK
G LINK
DAUGHTER CARDS
Each filling corresponds to a different flavor
TRANSITION CARDS
Each color corresponds to a different flavor
Created by Manuel F. Martin
May. 6. 99

General Overview

- Find positive/negative/isolated... CFT tracks in four Pt bins [1.5,3,5,10 GeV]
- Report 6 highest Pt tracks to the L1MUON
- Find CPSaxial and CPSstereo clusters
- Match CPSax clusters to CFT tracks
- Find FPS clusters in shower layers and match them with mip layer depositions
- In L1, report **counts** of various tracks (in Pt bins, ...), track/cluster matches, FPS clusters with/without mip layer to CTTT & FPTT, where neoterms are formed
- Upon L1 Accept (or "in L2"), report more detailed **lists of objects** to L2CFT, L2PS (axial & stereo), and L2FPS preprocessors
- Upon L1 Accept also report all of the inputs for the L1- Accepted events to the L3

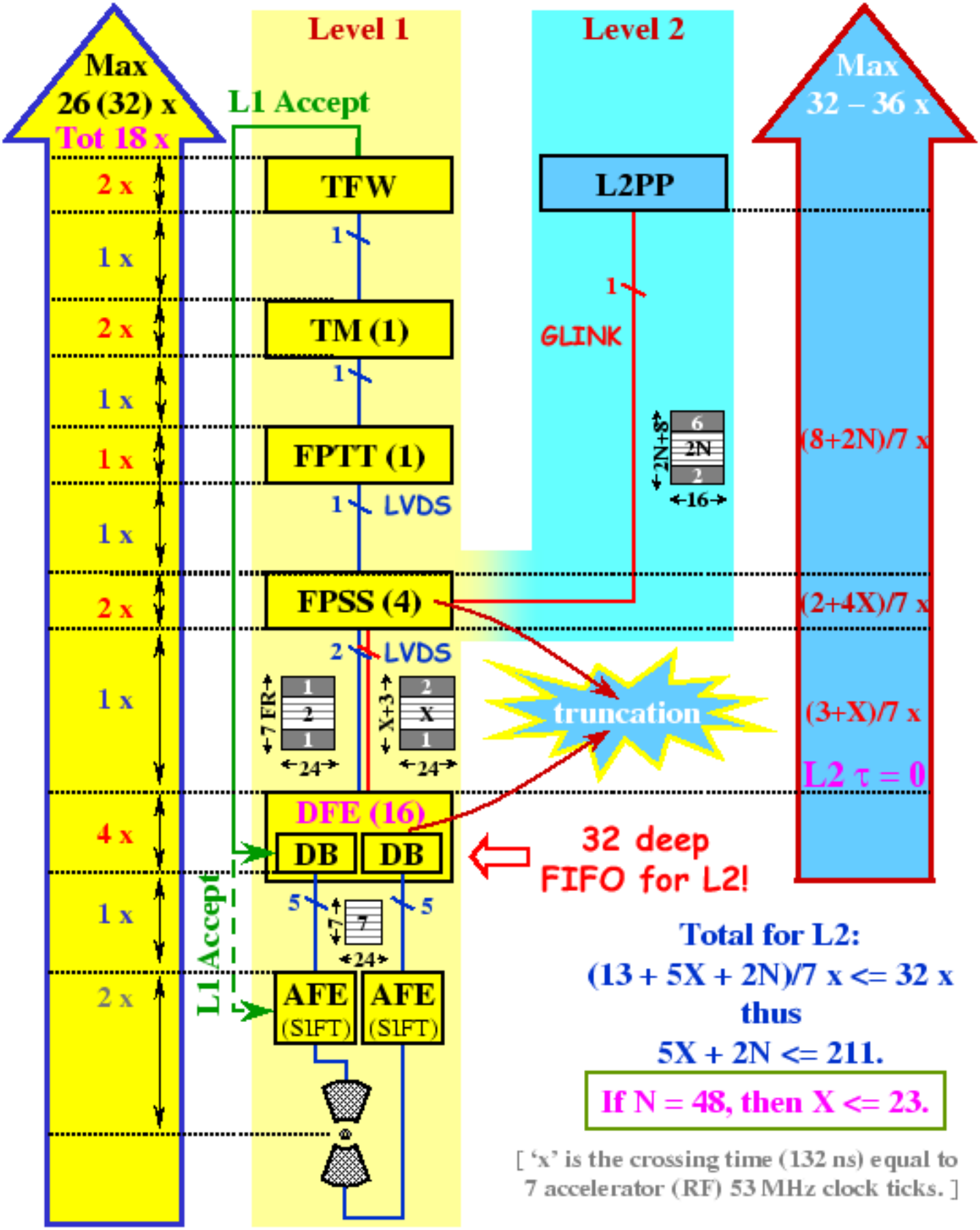
More Details… CFT/CPSax

- Normal, L1 Acquisition mode:
  - DFEA – In each of the 80 CFT/CPS sectors, find tracks, clusters, match them and report these **counts** to the collector boards, CTOC; Also send the 6 highest Pt tracks to L1MUON
  - CTOC – Sum up **counts** from 10 DFEAs, find isolated tracks in Octants, ...
  - CTTT – Based on the various **counts** from 8 CTOCs, form up to 96 neoterms (currently 64)
  - DFEA/CTOC/CTTT – maintain 32 events deep L1 Pipeline for inputs, and more ...
- Upon L1 Accept:
  - DFEA – Pull out the data for the corresponding event from the pipeline and either reprocess or send a **list** of tracks (up to 24) and clusters (up to 8) to CTOC
  - CTOC – Sort **lists** of tracks from 10 DFEAs in Pt and report up to 24 highest Pt tracks to CTQD
  - CTQD – Sort **lists** of tracks from 2 CTOCs in Pt and report up to 46 tracks to L2CFT
  - CTOC/CTTT – Send all of the inputs for the event that got L1-accepted to the L3 via G-Link


Level 1
Level 2
Max
26 (32) x
Tot 21 x
L1 Accept
TFW
L2CFT&PS
G-Link
TM (1)
FSCL
CTTT (1)
LVDS
CTQD (4)
CTOC (8)
truncation
DFEA (40)
SWDB
SWDB
To L1 MUON – 3x
MIXER (20)
AFE
(SIFT)
AFE
(SIFT)
L1 Accept
N = 46
X = 24
Max
32 – 36 x
(8+2N)/7 x
2x
(2+4X)/7 x
(3+X)/7 x
L2 τ = 0
2 x
1 x
2 x
1 x
1 x
1 x
3 x
1 x
4 x
1 x
1 x
1 x
2 x
LVDS
['x' is the crossing time (132 ns) equal to
7 accelerator (RF) 53 MHz clock ticks.]

More Details… FPS

- **Normal L1 Acquisition mode:**
  - DFEF – In each of the 32 FPS sectors, find clusters in 144 U and 144 V shower layer strips, match them with the upstream/mip layer deposition, and report **counts** of various types of clusters to FPSS
  - FPSS – Sum up **counts** from 8 DFEFs and report them to FPTT
  - FPTT – Based on the various **counts** from 4 FPSSs, form up to 96 neoterms (currently 32)
- **Upon L1 Accept:**
  - DFEF – Pull out the data for the corresponding event from the L1 pipeline and either reprocess or send a **list** of clusters (up to 24, 12 in U and 12 in V) to CTOC
  - FPSS – Out of 8 **lists** of 24 clusters report up to 48 U & V clusters to L2FPS; Select clusters such as to minimize any bias in azimuth
  - DFEF/FPSS/FPTT – Send all of the inputs for the event that was L1– accepted to the L3 via G-Link


Level 1
Level 2
Max
26 (32) x
Tot 18 x
L1 Accept
TFW
L2PP
TM (1)
GLINK
FPTT (1)
LVDS
FPSS (4)
LVDS
truncation
DFE (16)
DB
DB
32 deep
FIFO for L2!
L1Accept
AFE
(SIFT)
AFE
(SIFT)
Max
32 – 36 x
(8+2N)/7 x
(2+4X)/7 x
(3+X)/7 x
L2 τ = 0
2 x
1 x
2 x
1 x
1 x
2 x
1 x
4 x
1 x
2 x
Total for L2:
(13 + 5X + 2N)/7 x <= 32 x
thus
5X + 2N <= 211.
If N = 48, then X <= 23.
['x' is the crossing time (132 ns) equal to
7 accelerator (RF) 53 MHz clock ticks.]

More Details… CPSst

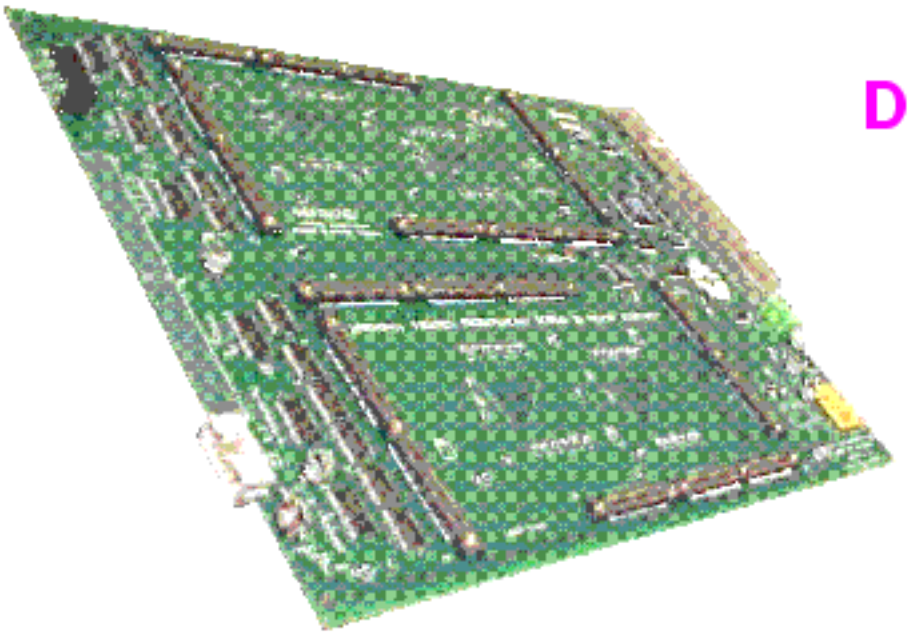
- **Normal, L1 Acquisition mode:**
  - DFES – Receive trigger output of 1280 NU, NV, SU, SV strips and store them in the L1 Pipeline
  - Note: CPSst not part of the L1 Trigger
- **Upon L1 Accept:**
  - DFES – Pull out the data for the corresponding event from the pipeline and start finding clusters; report a **list** of up to 16 (?) clusters from each of the four DFESs to L2PS
  - Very challenging is to handle the large number of strips but have enough time (is part of L2 only) and this saves the day

Some General Issues

- Run at RF clock ~ 53 MHz
- Need to synchronize all input records in all FPGAs as the data records can be skewed by over ± 1 RF clock cycle
- Receive all data, correct for single-bit transmission errors, re-map, and present the data to the processing algorithm
- Format the output according to the protocols to transfer on either LVDS, G-Link, or FSCL
- Implement 32-event-deep L1 pipeline
- Send all inputs to the L3 upon L1 Accept

DFE Hardware

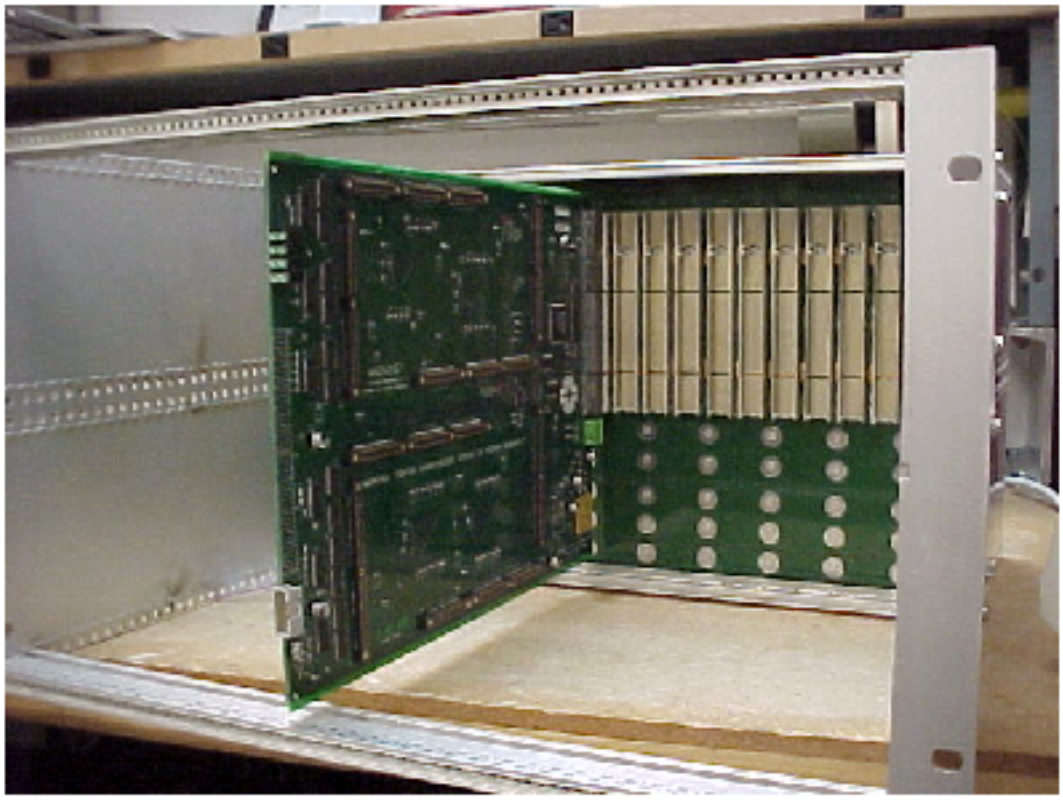
DFE Hardware (1)



DFE MotherBoard
Revision A

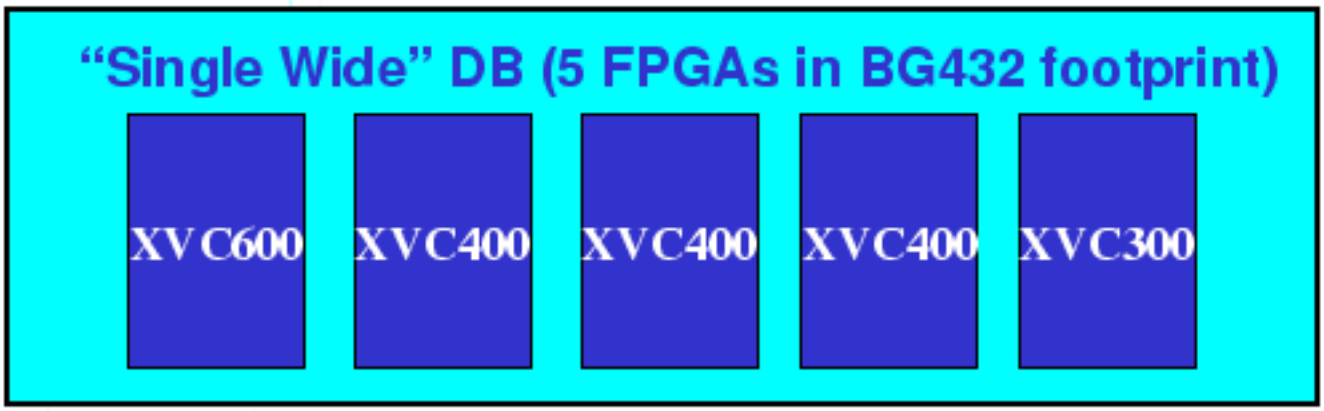
Uniform throughout the system

Front view of a DFE sub-rack with custom backplane and a DFE MotherBoard installed

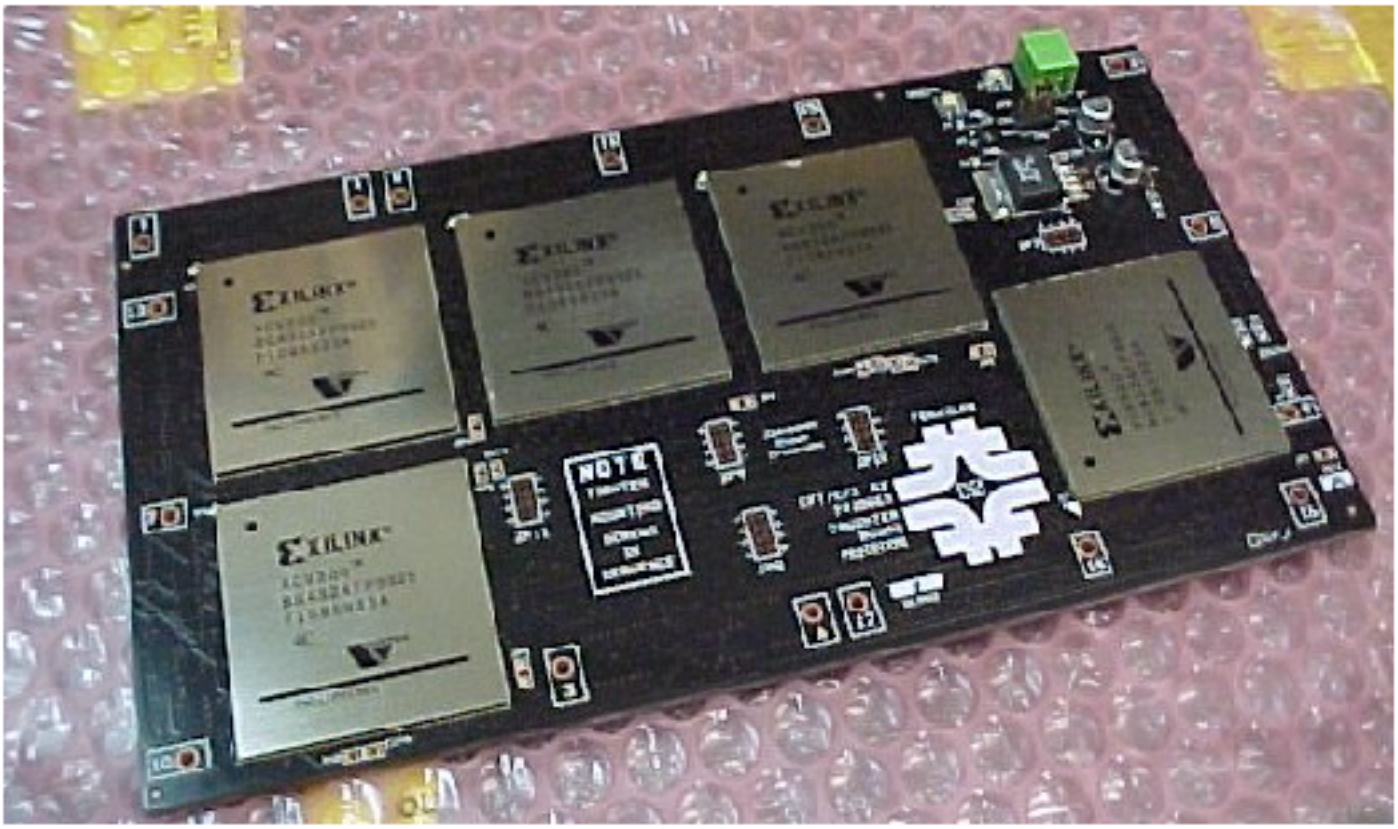


DFE Hardware (2)

- Two flavors of daughterboards, the so called "Single-Wide" and "Double-Wide"

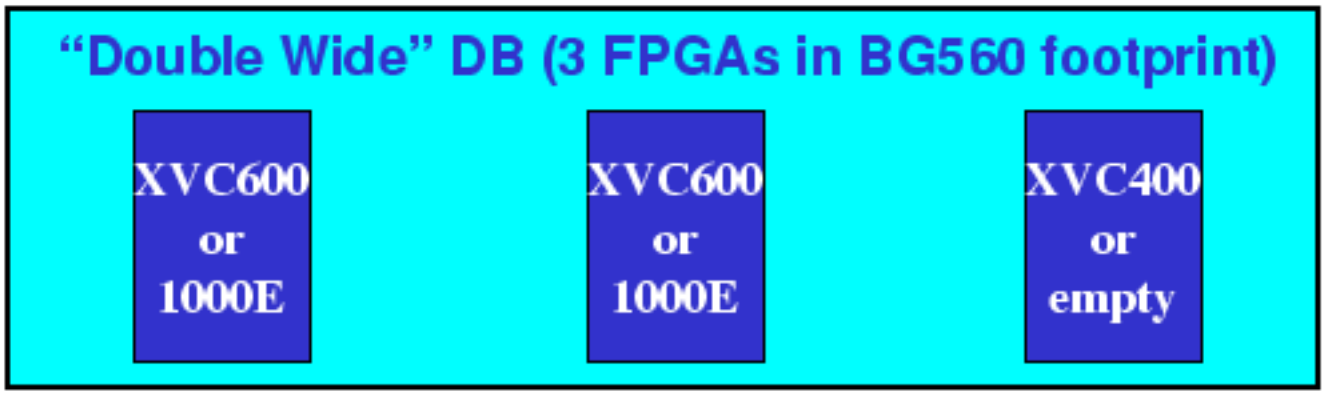


- "Single-Wide" used in DFEA only

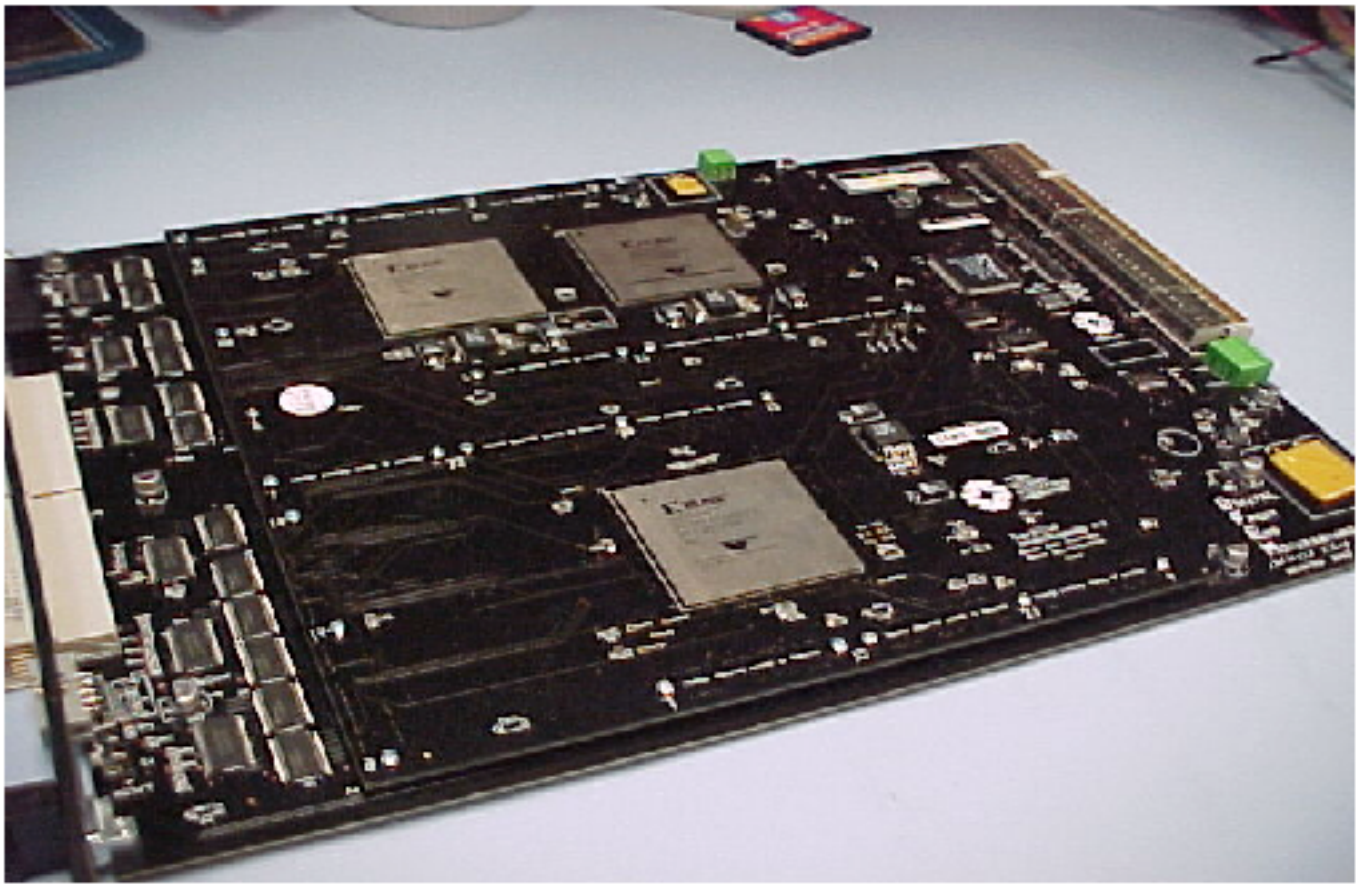


DFE Hardware (3)

- Two flavors of daughterboards, the so called "Single-Wide" and "Double-Wide"



- "Double-Wide" used in everything else



DFE Hardware (4)

- Xilinx Virtex FPGAs throughout the system
  - XCV400 – 0.5M gates, XCV1000E – 1.5M gates
  - Same footprint but different sizes allows a lot of flexibility in board/layout design
  - Each FPGA has 4 global clock and ~22 secondary clock nets; important for synchronization
  - Large dual-port memories; important for synchronization and pipelining of events
  - Xilinx FPGAs extremely cost-effective

DFE Hardware (5)

- All motherboards here and tested
- Mixers expected by the end of September
- All 80+8 DFEA daughterboards here
  - 40 are attached to 20 motherboards, out of which 16 are installed in the platform, and 11 are at PREPs with minor problems
- 2 CTOC and 1 CTQD daughterboards here, tested, and mounted on motherboards
- 6 new CTOCs here, final fabrication at the highrise, to be tested this week
- If successful, orders for fabrication of the remainder of CFT/CPSax and FPS chains goes out, due back in 4- 5 weeks
- Extremely bad "luck" with placing FPGAs on double-wides, have 9 at hand that need to be reworked, order is out
- Few remaining FPGAs for CPSst and STT boards due in 2 – 5 weeks, but not on the critical path
- Goal: DFE installed in October shutdown

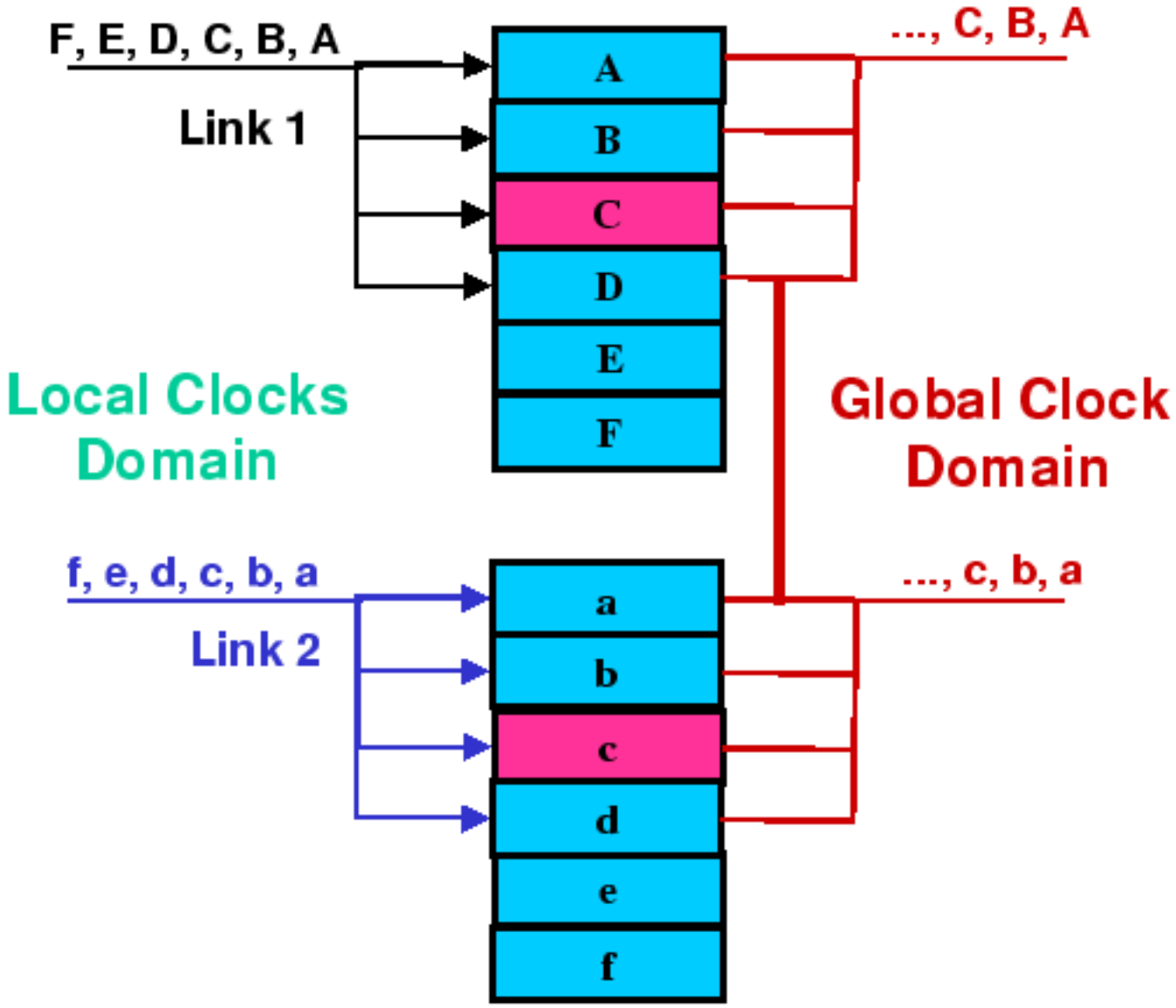
Firmware

VHDL

- Offshoot of the *Very High Speed Integrated Circuits* (VHSIC) founded by Department of Defense in late 1970s and early 1980s
- Describing complex integrated circuits with hundreds of thousands of gates was however very difficult using only gate level tools
- A new **hardware description** language was proposed in 1981 called *VHSIC Hardware Description Language*, or VHDL
- In 1986, VHDL was proposed as IEEE standard and after a number of revisions as the IEEE 1076 standard in 1987
- In some ways it is like a high level programming language but in *many* ways it is very different
- Most of the people including myself did not know any VHDL until Xilinx/Aldec FNAL Class just little over a year ago...
- I will review just a few of many examples of algorithm implementation in VHDL

Synchronization (L1FE)

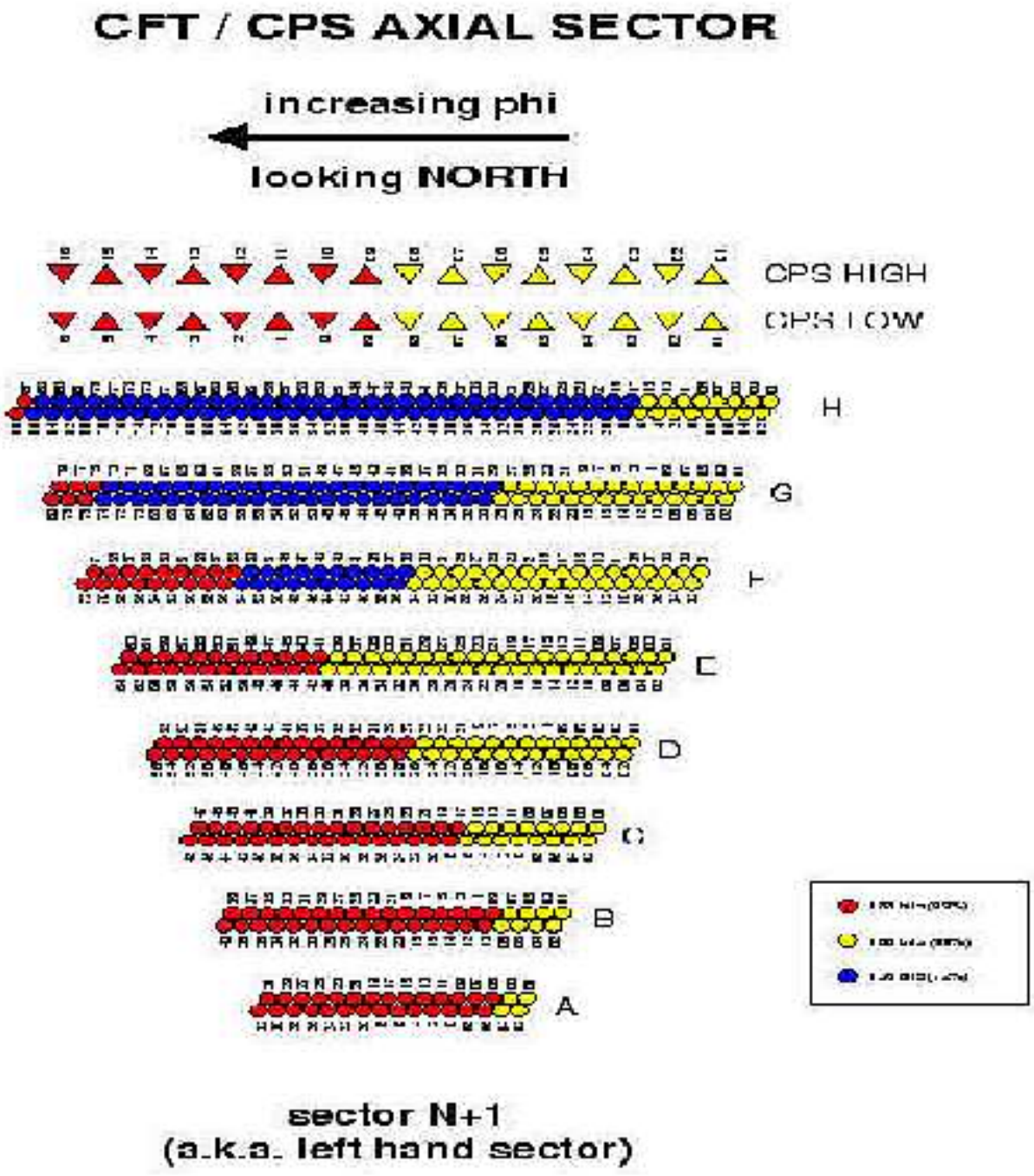
- Data are badly skewed at the inputs
- Synchronize using dual port memories



- Start reading out DPMs with Global Clock few ticks (currently 3) after earliest input
- Released & documented DØ Note 3881

DFEA Firmware (1)

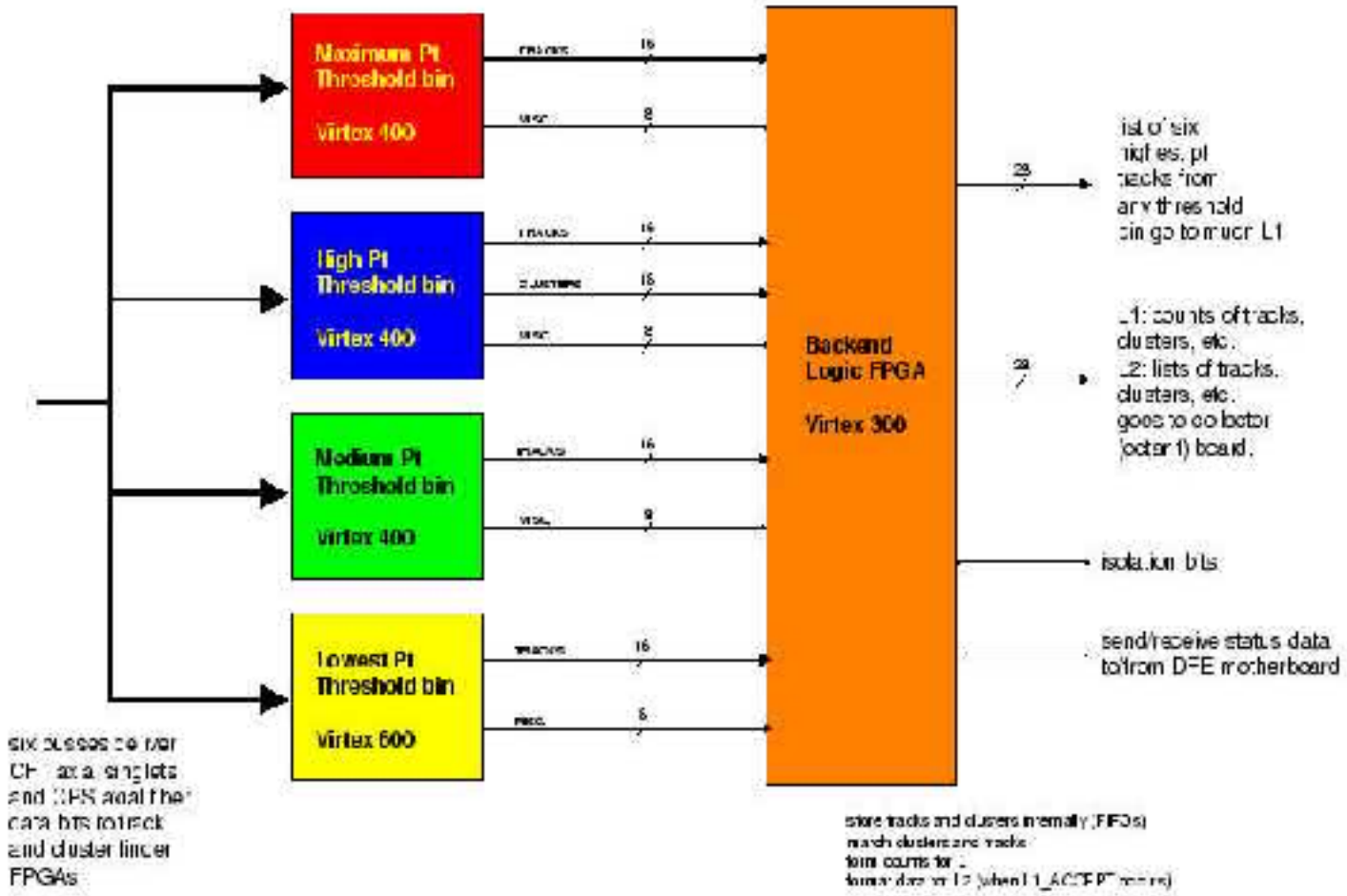
- Finds CFT tracks from CFT doublet hits in 4 Pt bin each with 4 sub-bins; In the lowest bin there are ~8,000 track equations



DFEA Firmware (2)

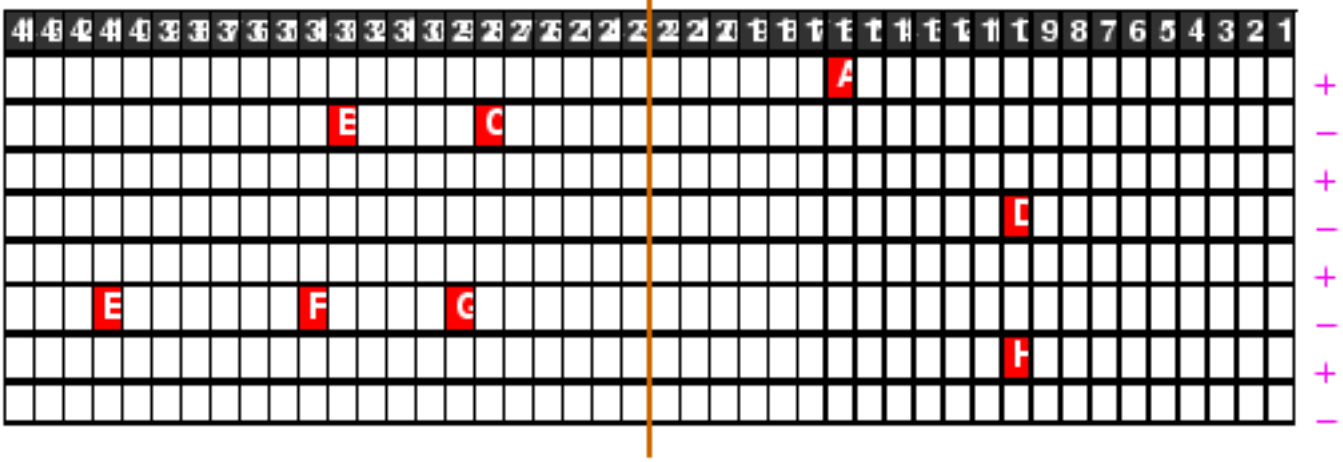
- Finds CFT tracks in four FPGAs, one per each Pt bin
- Finds CPS clusters; Does track/cluster matching in the backend FPGA, reports counts in L1 and more detailed lists of tracks & clusters in L2; Also reports 6 highest Pt tracks to L1MU

CFT/CPS AXIAL Trigger Daughter Board Dataflow



DFEA Firmware (3)

- In each Pt bin, track equations are represented as a two dimensional array 44 wide (phi) and 8 tall (±4 sub-bins).



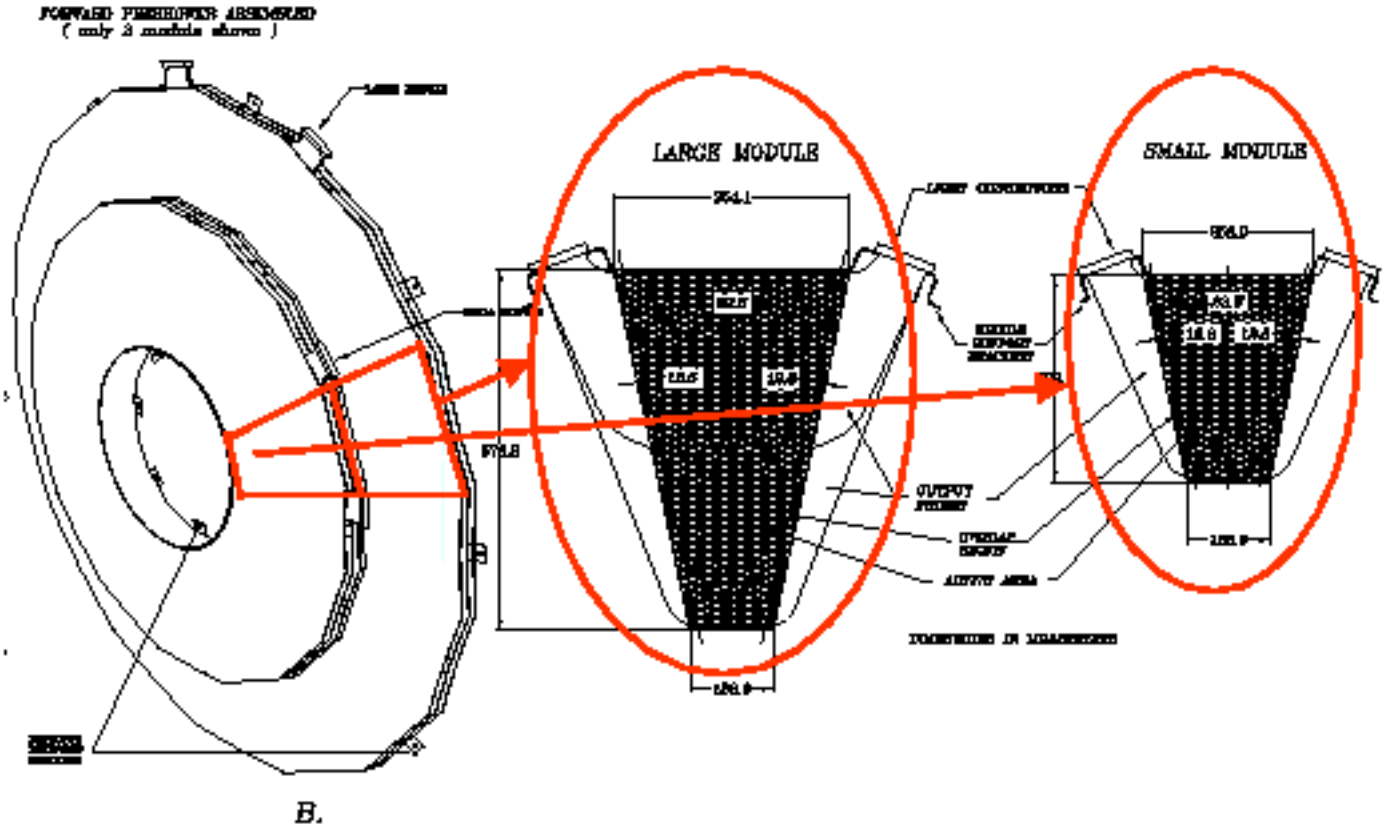
- In the above array, 8 tracks are found, however, only six tracks are reported as follows:
  - Track A is reported.
  - Track B is reported, C is pushed on the stack.
  - Track D is reported
  - Track E is reported, G is pushed on the stack, F is Lost.
  - Track H is reported.
  - Track G is popped from the stack and reported. Stack is then cleared.

DFEA Firmware (4)

- CPSax cluster finder sees 16 strips from the homesector and 8 strips from previous and next neighboring sector
- It finds 6 clusters in each of the two 16-strip halves
- Depending on the Pt bin of a CFT track, it is extrapolated out to CPSax radius
- If the extrapolated CFT track passes within number of strips of the CPS cluster centroid, the track and cluster are considered to be matched; the size of the matching "window" is Pt bin dependent
- DFEA also calculates the number of doublet hits in the sector and this is used in Hit / Occupancy Level Trigger

DFEF Firmware (1)

16 FPS 22.5° φ-sectors
4 layers of U- & V-strips



B.

Shower: 144 U & V-strips
Mip: 103 U & V-strips
Special: 72 U & V-strips

Total max ~ 500 analog signals per FPS φ-sector

DFEF Firmware (2)

- Receives L1 FPS data – trigger bits in U and V layers in the 103 upstream/Mip strips and the 144 downstream/Shower strips
- In L1, count the number of U / V "electron" and "photon" candidates and report four counts per each orientation to the FPSS
- In L2, i.e. upon the L1 Accept, report clusters (max 24) to FPSS introducing as minimal bias as possible in truncating clusters in 144 U+V strips down to 24. Need eta-phi matching of some sort to report at least one U-V match per CAL Trigger Tower (~12 covered by FPS)
- In what follows, I'd like to describe the cluster finder implemented in VHDL and compare it to the possible implementation in C++

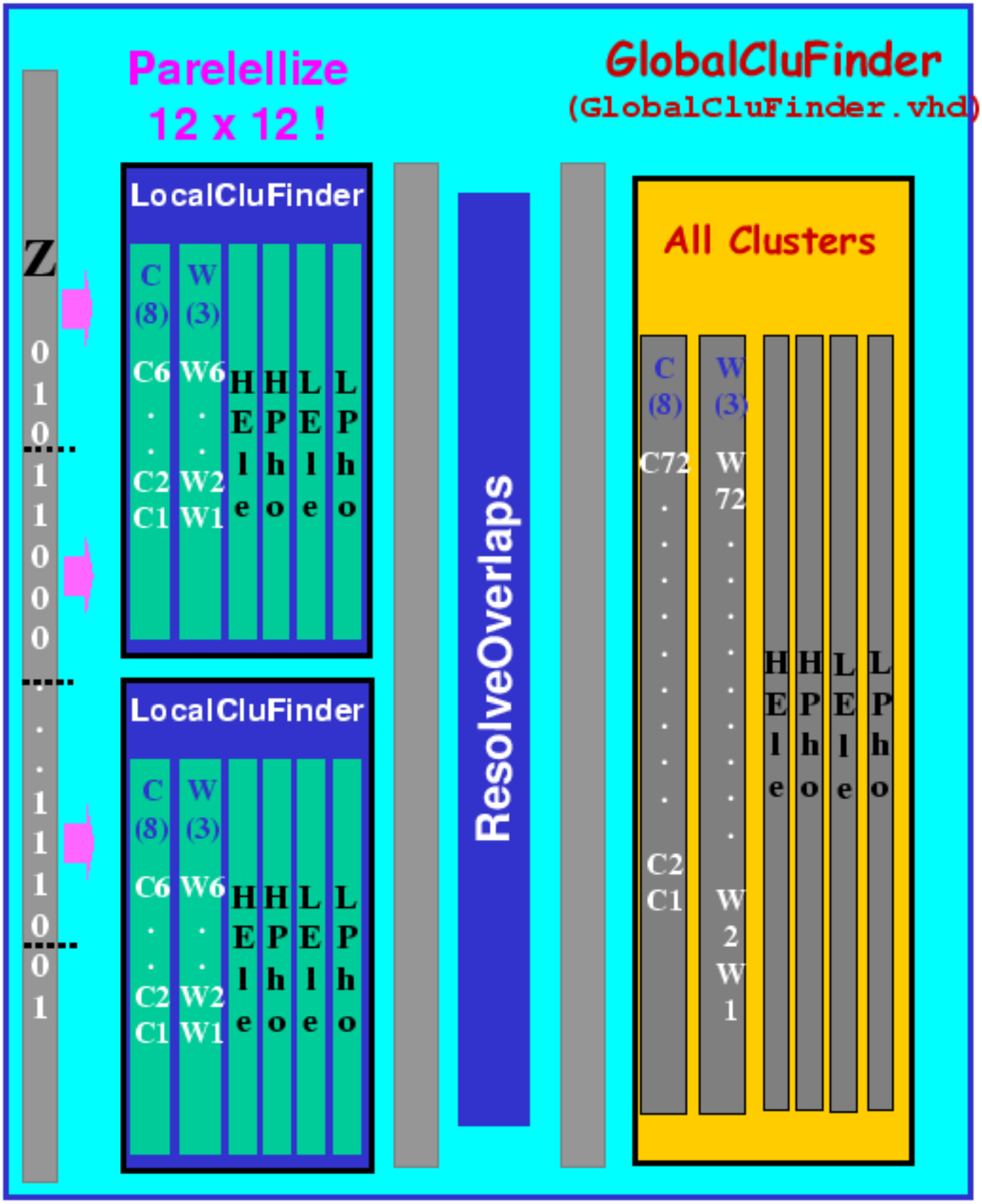
DFEF Firmware (3)

- The cluster finder code in C++ can be quite simple

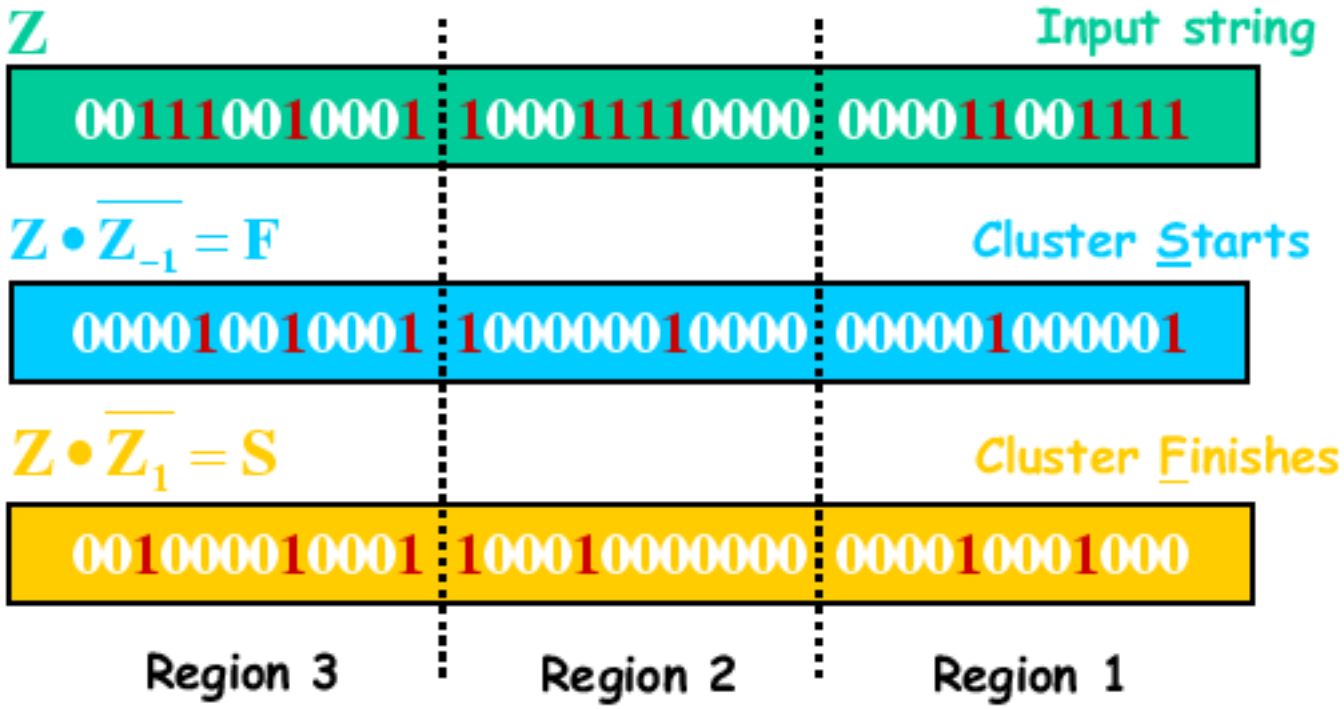
```
void FPSWedge::CluFind()
{
  int IStrip; int NewCluster=1;
  for( IStrip=1;IStrip<=N_SHO;IStrip++ ){
    if ( ShoL[IStrip]==1 ){
      if ( NewCluster==1 ){
        NewCluster = 0;
        NClu++;
        CluSta[NClu] = IStrip;
        CluWid[NClu] = 1;
      }
      else if ( NewCluster==0){
        CluWid[NClu]++;
      }
    }
    else if ( NewCluster==0 ){
      NewCluster = 1;
    }
  }
}
```

- Let's see how it can be done in VHDL...

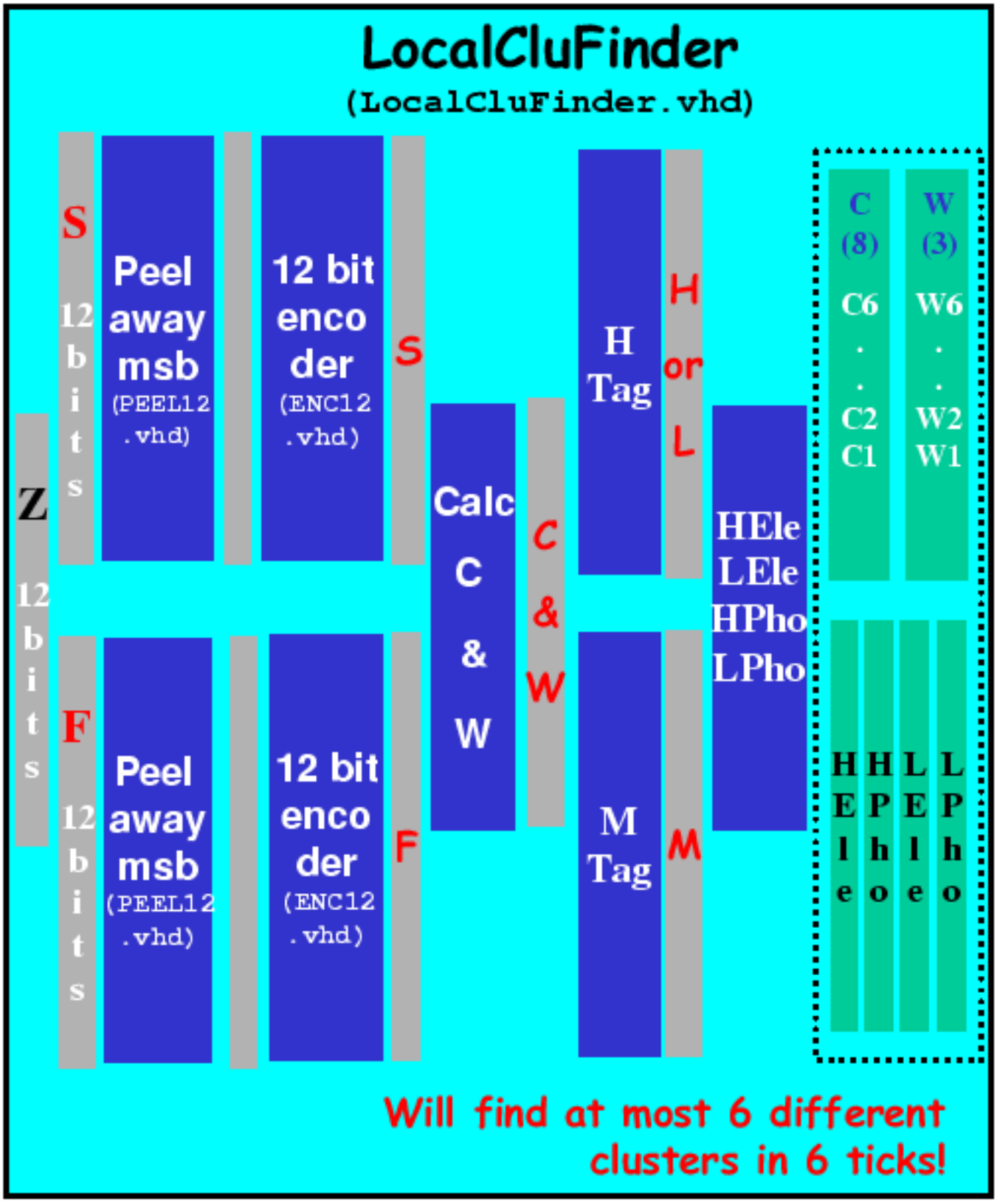
DFEF Firmware (4)



DFEF Firmware (5)



DFEF Firmware (6)

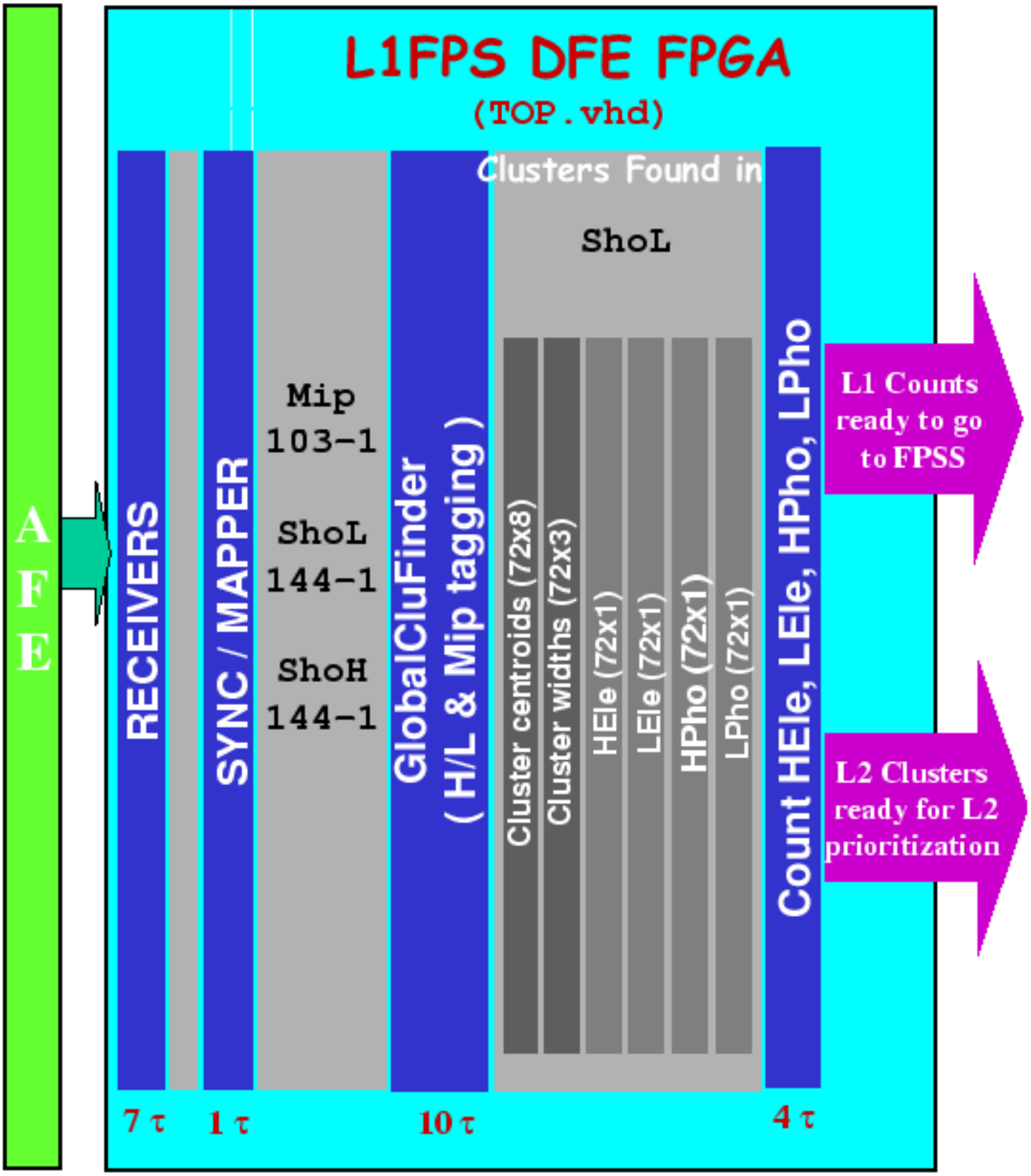


DFEF Firmware (7)

➢ A sample of VHDL process for MIP tagging

```
Process( Clock )
Begin
If ( Clock'event and Clock = '1' ) Then
  If ( Centr = ShoEnR-0  ) Then
    MMask <= M(ShoEnR-0+6  downto ShoEnR-0);
  ElsIf ( Centr = ShoEnR-1  ) Then
    MMask <= M(ShoEnR-1+6  downto ShoEnR-1);
  ...
  ElsIf ( Centr = ShoEnR-11 ) Then
    MMask <= M(ShoEnR-11+6 downto ShoEnR-11);
  Else
    MMask <= "0000000";
  End If;
  --
  If ( MMask(7) = '1' or MMask(6) = '1' or
       MMask(5) = '1' or MMask(4) ='1' ) Then
    Mbit <= '1';
  ElsIf ( MMask(3) = '1' or MMask(2) = '1' or
          MMask(1) = '1' ) Then
    Mbit <= '1';
  Else
    Mbit <= '0';
  End If;
End If;
End Process;
```

DFEF Firmware (8)



Firmware vs. Software ?

- Sorting 10 lists of 24 tracks in order to report 24 highest Pt tracks e.g. in L2CTOC takes on the order of 30 RF clock ticks, or approximately **500*ns***
  - Rough estimation of a similar task of sorting *N* objects in software goes at best as $N\log_2 N$ and with four 1*ns* cycles per each of *N* basic operation gives ~ **7500*ns***, an order of magnitude more...

- Cluster finding in 144 FPS U & V strips, ***regardless*** of cluster pattern, takes 8 RF clock ticks or approximately **150*ns***
  - Rough estimation of a similar task in software, assuming "...101010..." pattern, goes as $4*N/2 + 7*N/2 = 11*N/2$ (in *ns*) with *N* being the total number of strips. This gives for U & V cluster finding 11*144 ~ **1600*ns***, again about an order of magnitude more...

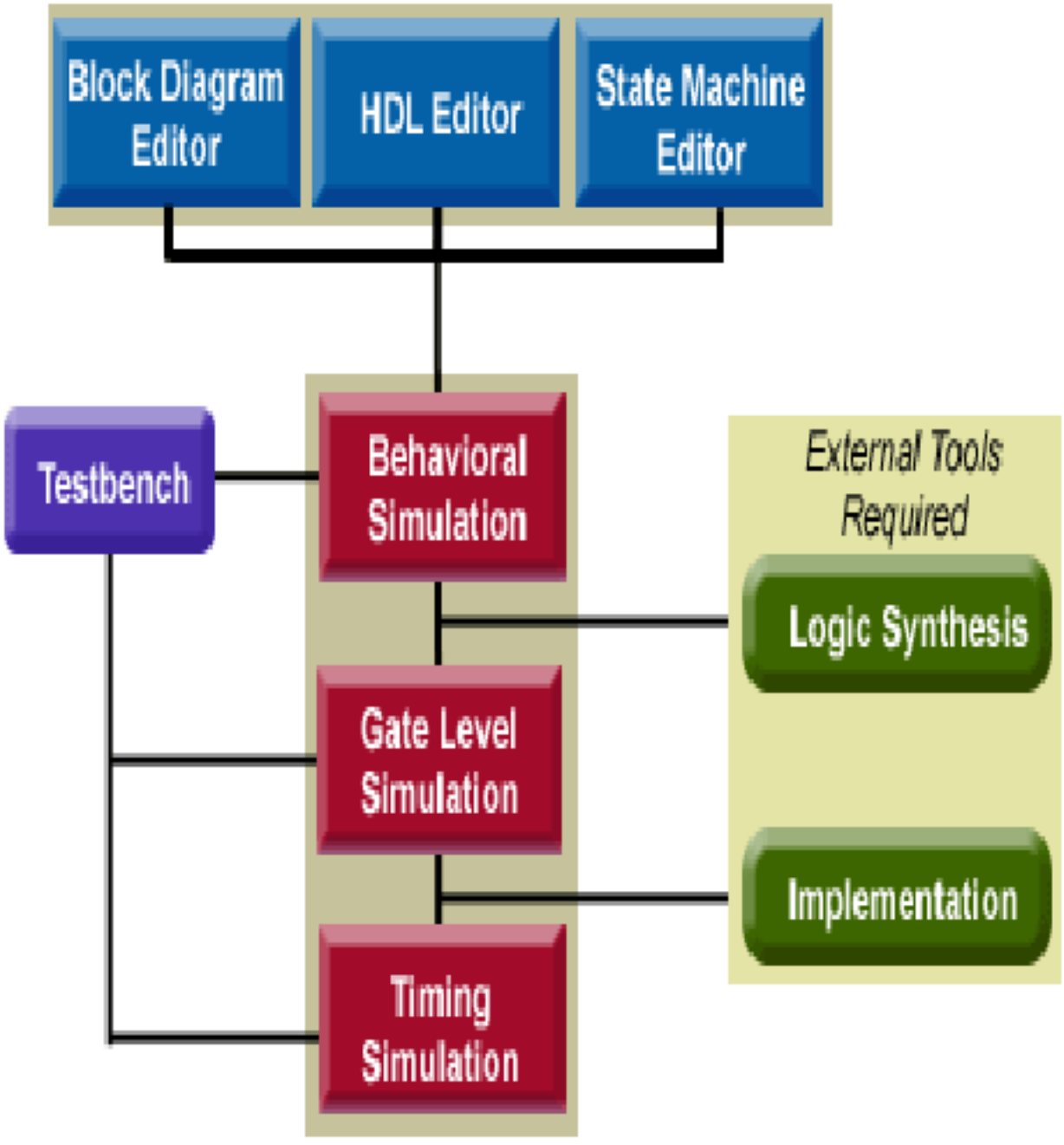
Firmware Certification

- Design algorithms for board / functionality
- Write VHDL code, pipelined design
- Behavioral Simulations: SoftBench, Test-Vectors
- Synthesis/constraints (GCkl buffers, clock to out,...)
- Implementation/constraints (board layout, clocks, skews on nets, etc.), resources, speed
- Timing Simulations: same SoftBench, Test-Vectors (!)
- TestStand – download in target hardware and run with the same TestVectors (!)
- Board/Functionality certified
- SoftBench for multi-board/FPGA chain, propagate TestVectors
- Chain TestStand with the same Test-Vectors
- Firmware certified

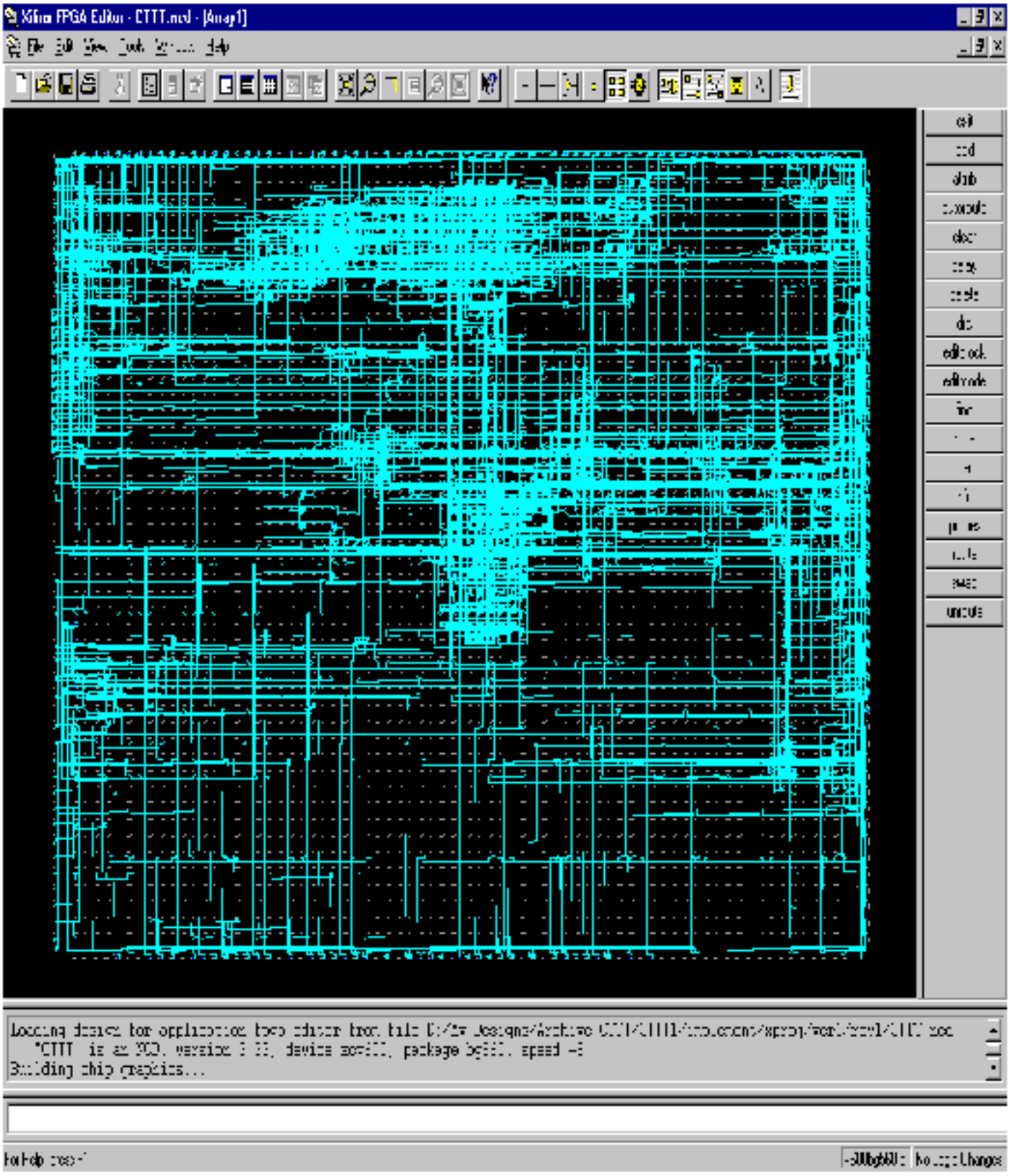
Firmware TestBench

Active-HDL™

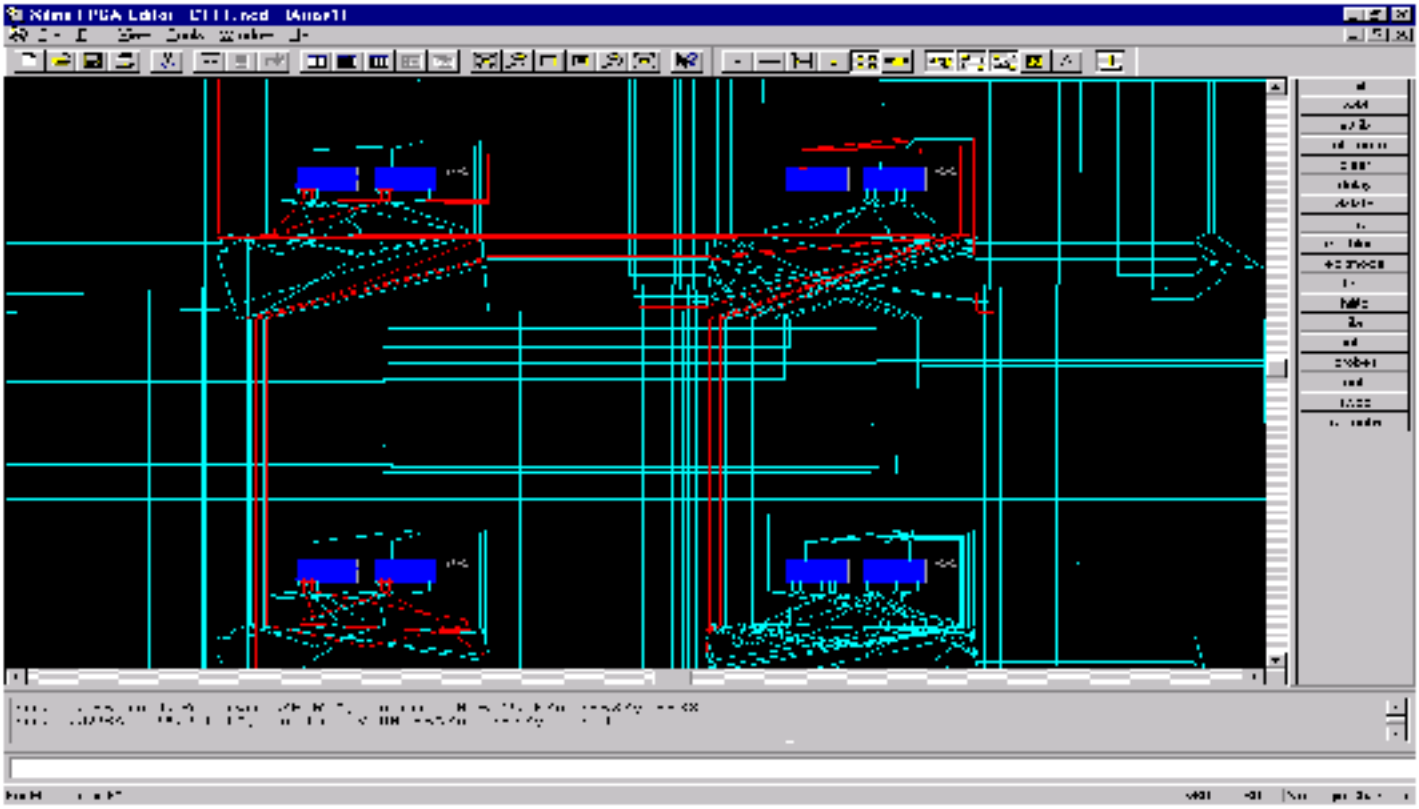
Complete FPGA Verification Environment

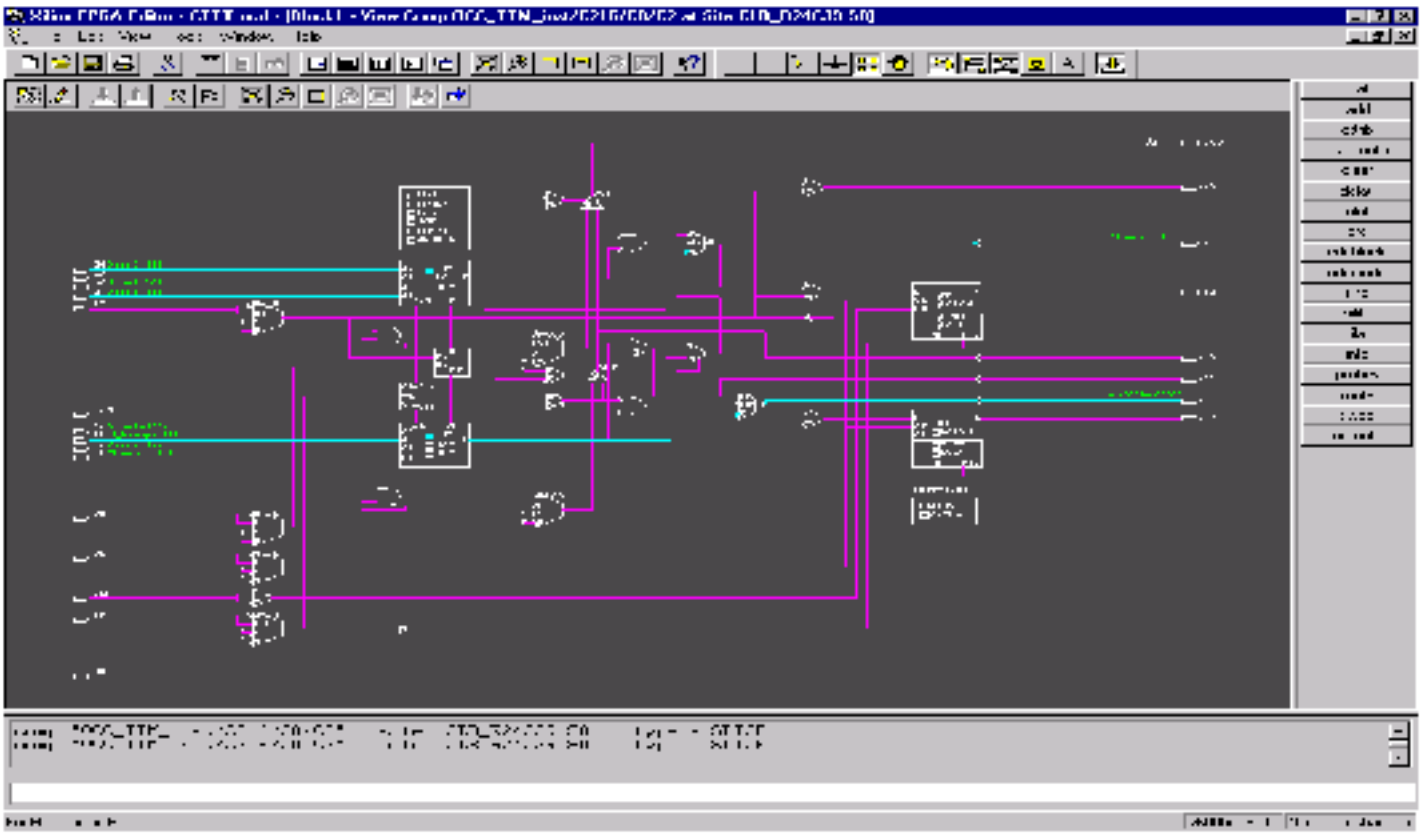


Firmware Implementation (1)



Firmware Implementation (2)



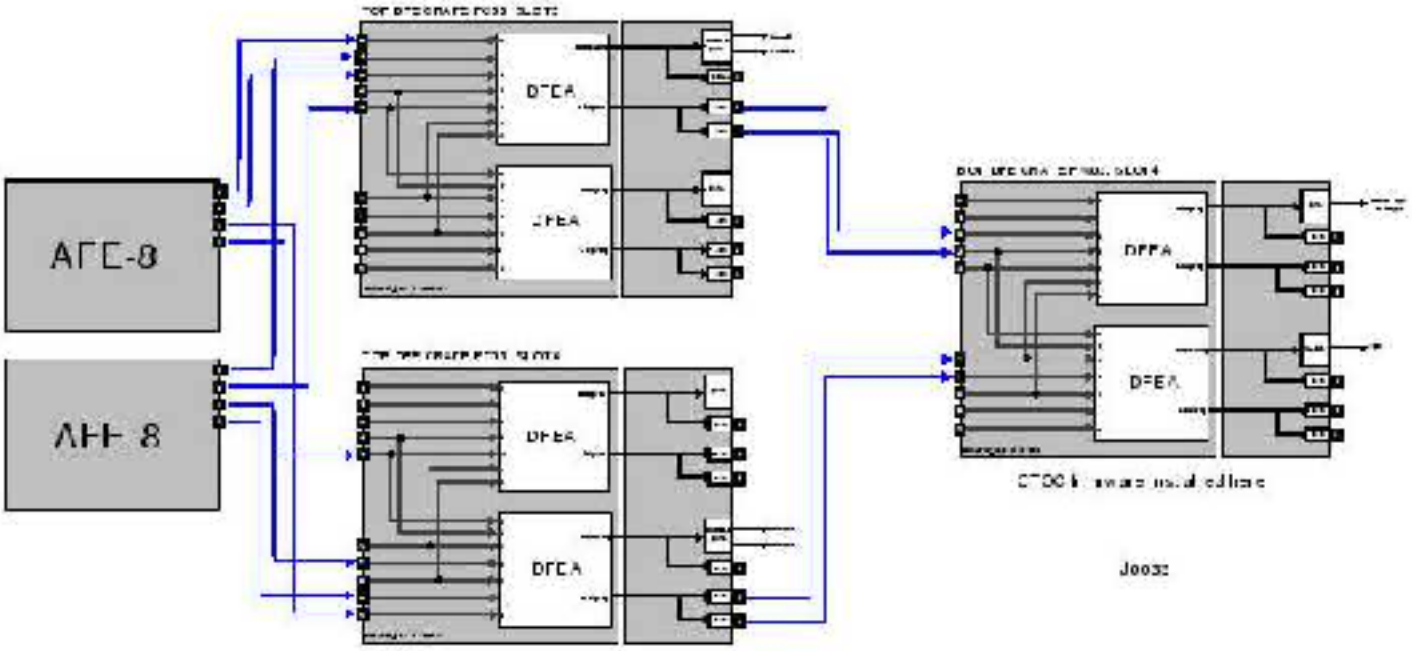


Status and Plans

All DØ Meeting, August 3, 2001, Fermilab Levan Babukhadia

Hit / Occupancy Trigger

- Due to hardware limitations, decided to set up only CFT Hit / Occupancy Trigger
- Three neoterms are provided with tunable threshold values on doublet counts
- Have in the platform 2 AFEs, 2 DFEAs, and one surrogate CTOC. The latter implements CTOC plus some of CTTT functionality



- AFE → DFEA chain working, adding CTOC
- Full TestStand being assembled in DAB
- Download software Ok for Single-Wides, in works for Double-Wides

Near / Future Term Plans

- Biggest milestone is to have all AFE and DFE hardware installed during the October shutdown
- Schedule is tight for AFEs as well as for DFEs; If worst comes, should still have at least CFT/CPSax instrumented
- Hit/Occupancy trigger firmware in place and is being now commissioned ~2 weeks
- Large number of L1 firmware pieces exists
  - DFEA, CTOC, CTTT need hardware tests
  - DFEF, FPSS, FPTT individually passed hardware tests last year and worked in chain simulations
  - General synchronization firmware in place
  - General L1→ L3 Sender firmware in place
- Firmware for L2 in worse shape
  - DFEA, CTOC, DFEF, and FPSS all need major work on L1 pipelining and L2 reporting
  - On the other hand, CTQD is in good shape, needs to be commissioned in the hardware next, and we expect DFES to start commissioning in about a month

Thanks to Many People

Of course many people's hard work makes a project like this happen and I would like to thank them all, especially ones from DFE group (apologies if I overlooked anyone)

Mrinmoy Bhattacharjee

Jerry Blazey

Fred Borcherding

Brian Connolly

Satish Dasei

Paul Grannis

Juan Lizarazo

Arnaud Lucotte

Steve Lynn

Manuel Martin

Jamieson Olsen

Ricardo Rodrigez

Qichun Xu

Kin Yip

...

Concluding Remarks

- L1 CTT digital trigger is truly unique in the experiment as it is heavily based on reprogrammable devices for both physics algorithms as well as for solving hardware issues (such as e.g. synchronization)
- It is therefore an extremely flexible organism allowing continual improvement and development of algorithms as we go along, provided that we have the hardware
- Many issues are still open, such as storage of firmware downloadables and versioning but we are talking to our computing experts and are considering possible solutions
- Even though we are turning on slowly, with only Hit Trigger, we will be evolving to a full capability especially if hardware problems are resolved
- Stresses importance of Trigger emulation
- Extensive testing of firmware using good set of TestVectors and a TestBench is vital